

**LIST OF PRIOR ART CITED BY
APPLICANT
(PTO-1449)**

ATTY. DOCKET NO.
Intel-0044

APPLN. SERIAL NO.
**New U.S. Patent
Application**

APPLICANT(S): Stephen TANG, Ali KESHAVERZI, Dinesh
SOMASEKHAR, Fabrice PAILLET, Muhammad KHELLAH,
Yibin YE, Shih-Lien LU, Vivek DE

FILING DATE
November 26, 2003

GROUP
N/A 2827

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	*PATENT NO.	*ISSUE DATE	*INVENTOR NAME	CLASS	SUBCLASS	FILING DATE

U.S. PATENT APPLICATION PUBLICATIONS

	*PATENT APPLN. PUB. NO.	*PUB. DATE	*APPLICANT	CLASS	SUBCLASS	

U.S. PATENT APPLICATIONS

	*APPLN. NO.	*FILING DATE	*INVENTOR	CLASS	SUBCLASS	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Publisher, Place of Publication, Etc.)

HHA	S. Okhonin et al.; A SOI Capacitor-less IT-DRAM Concept; October 2001; pgs. 153-154; 2001 IEEE International SOI Conference		
	Charles Kuo et al.; A Capacitorless Double-Gate DRAM Cell; June 2002; pgs. 345-347; IEEE Electron Device Letters, Vol. 23, No. 6		
HHA	Takashi Ohsawa et al.; Memory Design Using a One-Transistor Gain Cell on SOI; Nov. 2002; pgs. 1510-1522; IEEE Journal of Solid-State Circuits, Vol. 37, No. 11		
	Takashi Ohsawa et al.; A Memory Using One-Transistor Gain Cell on SOI (FBC) with Performance Suitable for Embedded DRAM's; 2003 Symposium on VLSI Circuits Digest of Technical Papers		
HHA	Takashi Ohsawa et al.; ISSCC 2002/ Session 9/ Dram and Ferroelectric Memories/ 9.1		
EXAMINER	Huan Hoang	DATE CONSIDERED	5/12/05

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.